UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,916	03/22/2004	William R. Hancock	H0006326--1623	3884

128 7590 03/13/2006

HONEYWELL INTERNATIONAL INC.
101 COLUMBIA ROAD
P O BOX 2245
MORRISTOWN, NJ 07962-2245

EXAMINER	
HSU, JONI	
ART UNIT	**PAPER NUMBER**
2671	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/806,916	HANCOCK, WILLIAM R.
	Examiner	Art Unit
	Joni Hsu	2671

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/12/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on December 12, 2005 was filed after the mailing date of the application on March 22, 2004. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

2. In light of Applicant's amendments to the specification and to Claim 5, the objections to the specification and to Claim 5 have been withdrawn.

3. Applicant's arguments filed December 19, 2005 have been fully considered but they are not persuasive.

4. With regard to Claims 1-9, 11-21, and 23-28, Applicant argues that Barilovits (US 20020145610A1) does not disclose a linear-output gamma translator (page 11).

In reply, the Examiner disagrees. Barilovits describes translation from RGB to R'G'B' [0232] to YCbCr [0018]. The translation from RGB to R'G'B' is a non-linear transformation from a non-gamma corrected, non-linear space to a gamma corrected, non-linear space [0232]. Applicant agrees that R'G'B' is a non-linear gamma space, in page 11 of the remarks. Barilovits describes that the translation from R'G'B' to YCbCr is a linear transformation from a gamma

corrected, non-linear space to a gamma corrected, linear space [0018]. Therefore, the YCbCr output is a linear gamma space output, and therefore Barilovits does disclose a linear-output gamma translator.

Applicant argues that there is no teaching in Barilovits that the ODE renders a linear-gamma space output of a translator. While Barilovits does describe some non-linear output translation, it is not the translation of image data that has been previously translated into a linear gamma space and then rendered (pages 11-12).

In reply, the Examiner disagrees. Barilovits describes that the linear-output gamma translator outputs to the low pass filter [0235], which outputs to memory [0239], as can be seen in Figure 7, and the memory outputs to a processor core (overlay display engine), as can be seen in Figure 1, the processor core rendering the translated image data to create rendered image data (*overlay display engine reads memory buffers and merges with the graphics display in the primary display engine*, [0104], lines 9-11); and a non-linear-output translator, the non-linear-output translator translating the rendered image data into a non-linear gamma space (*compensates for the non-linear intensity function of a non-CRT display*, [0224], *after the computation of a graphics image is complete, gamma correction should be applied to the image prior to display to compensate for the monitor's non-linear voltage to intensity response*, [0015]).

5. With regard to Claims 10 and 22, Applicant argues that there is no description in Barilovits of a transformation to a linear-gamma space occurring during a memory read (page 12).

In reply, the Examiner disagrees. Barilovits describes that the linear-output gamma translator translates the received image data into a substantially linear gamma space (*data that has been non-linearly transformed by the gamma correction block is in an R'G'B' color space, the R'G'B' pixels produced by the gamma correction block are converted to YCbCr*, [0232], *YCbCr color spaces are derived from gamma corrected R'G'B' color spaces by a linear transformation*, [0018]). The linear-output gamma translator outputs to the low pass filter [0235], which outputs to memory [0239], as can be seen in Figure 7, and the memory outputs to a processor core (overlay display engine), as can be seen in Figure 1, the processor core rendering the translated image data to create rendered image data (*overlay display engine reads memory buffers and merges with the graphics display in the primary display engine*, [0104], lines 9-11).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-8, 10, 11, 14-19, 22-24, and 26-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Barilovits (US 20020145610A1).

8. With regard to Claim 1, Barilovits describes a graphics processor (computer graphics system, [0024]), the graphics processor receiving image data, the graphics processor comprising a linear-output gamma translator (RGB to YcbCr, Figure 7). Barilovits describes translation from RGB to R'G'B' [0232] to YCbCr [0018]. The translation from RGB to R'G'B' is a non-linear transformation from a non-gamma corrected, non-linear space to a gamma corrected, non-linear space [0232]. The translation from R'G'B' to YCbCr is a linear transformation from a gamma corrected, non-linear space to a gamma corrected, linear space [0018]. Therefore, the YCbCr output is a linear gamma space output. Therefore, Barilovits discloses a linear-output gamma translator, the linear-output gamma translator translating the received image data into a substantially linear gamma space. The linear-output gamma translator outputs to the low pass filter [0235], which outputs to memory [0239], as can be seen in Figure 7, and the memory outputs to a processor core (overlay display engine), as can be seen in Figure 1, the processor core rendering the translated image data to create rendered image data (*overlay display engine reads memory buffers and merges with the graphics display in the primary display engine*, [0104], lines 9-11); and a non-linear-output translator, the non-linear-output translator translating the rendered image data into a non-linear gamma space (*compensates for the non-linear intensity function of a non-CRT display*, [0224], *after the computation of a graphics image is complete, gamma correction should be applied to the image prior to display to compensate for the monitor's non-linear voltage to intensity response*, [0015]).

9. With regard to Claim 2, Barilovits describes that the linear-output gamma translator comprises a lookup table [0225, 0018].

10. With regard to Claim 3, Barilovits describes when the linear-output gamma translator is converting from R'G'B' to YCbCr, it adds bits [0018]. Therefore, the linear-output gamma translator additionally converts the received image data into a higher bit representation.

11. With regard to Claim 4, Barilovits describes that the higher bit representation comprises a floating point representation (*correct to three decimal places*, [0018], lines 17-25).

12. With regard to Claim 5, Barilovits describes that the non-linear-output gamma translator additionally converts the rendered image data into a lower bit representation [0032, 0033].

13. With regard to Claim 6, Barilovits describes that the received image data includes graphics data and video data [0024].

14. With regard to Claim 7, Barilovits describes that the received image data is received from a memory (*retrieves all of the parameters required to scale and filter an image from an attribute list in memory*, [0243]).

15. With regard to Claim 8, Barilovits describes that the linear-output gamma translator comprises a input translator, the input translator translating image data inputted into the graphics processor to a substantially linear gamma space [0232, 0018].

16. With regard to Claim 10, Barilovits describes that the linear-output gamma translator translates the received image data into a substantially linear gamma space (*data that has been non-linearly transformed by the gamma correction block is in an R'G'B' color space, the R'G'B' pixels produced by the gamma correction block are converted to YCbCr*, [0232], *YCbCr color spaces are derived from gamma corrected R'G'B' color spaces by a linear transformation*, [0018]). The linear-output gamma translator outputs to the low pass filter [0235], which outputs to memory [0239], as can be seen in Figure 7, and the memory outputs to a processor core (overlay display engine), as can be seen in Figure 1, the processor core rendering the translated image data to create rendered image data (*overlay display engine reads memory buffers and merges with the graphics display in the primary display engine*, [0104], lines 9-11). Since the transformation to a linear-gamma space occurs during a memory read, the linear-output gamma translator inherently comprises a memory read translator, the memory read translator translating image data read from a memory to a substantially linear gamma space. Barilovits describes that the non-linear-output gamma translator comprises a memory write gamma translator, the memory write gamma translator translating image data written to the memory to a non-linear gamma space (*destination memory management that packs image data into convenient formats for outputting to display devices*, [0036], *non-linear intensity function of a non-CRT display, such as an LCD screen*, [0224]).

17. With regard to Claim 11, Barilovits describes that the non-linear gamma space representation comprises a gamma of approximately .45 (*standard gamma correction exponent is 0.45*, [0014]).

18. With regard to Claim 14, Bariloivits describes a method for rendering received image data in a graphics processor (*computer graphics system, process 2-D and 3-D computer graphics images*, [0024], the method comprising the steps of translating the received image data to a substantially linear gamma space [0232, 0018]; rendering the translated image data to create rendered image data [0104]; translating the rendered image data to a non-linear gamma space; and outputting the non-linear gamma space rendered image data for display [0224, 0015].

19. With regard to Claim 15, Claim 15 is similar in scope to Claim 2, and therefore is rejected under the same rationale.

20. With regard to Claim 16, Claim 16 is similar in scope to Claim 3, and therefore is rejected under the same rationale.

21. With regard to Claim 17, Claim 17 is similar in scope to Claim 5, and therefore is rejected under the same rationale.

22. With regard to Claim 18, Claim 18 is similar in scope to Claim 6, and therefore is rejected under the same rationale.

23. With regard to Claim 19, Claim 19 is similar in scope to Claim 7, and therefore is rejected under the same rationale.

24. With regard to Claim 22, Claim 22 is similar in scope to Claim 10, and therefore is rejected under the same rationale.

25. With regard to Claim 23, Barilovits describes a graphics processor, the graphics processor receiving image data [0024], the graphics processor comprising an input gamma translator, the input gamma translator translating the received image data into a substantially linear gamma space and a higher bit representation [0232, 0018]; a processor core, the processor core rendering the translated image data to create rendered image data [0104]; and an output gamma translator, the output gamma translator translating the rendered image data into a non-linear gamma space output video data to a non-linear gamma space [0224, 0015] and a lower bit representation [0032, 0033]; a memory write gamma translator (destination memory management), the memory write gamma translator translating image data written to a memory to a non-linear gamma space and a lower bit representation (*destination memory management that packs image data into convenient formats for outputting to display devices*, [0036], *non-linear intensity function of a non-CRT display, such as an LCD screen*, [0224, 0032, 0033]); and a memory read gamma translator (color promotion) translating image data read from the memory to a substantially linear gamma space and a higher bit representation [0028, 0029].

26. With regard to Claim 24, Barilovits describes that the input gamma translator and the output gamma translator comprise a lookup table [0223, 0225].

27. With regard to Claim 26, Claim 26 is similar in scope to Claim 4, and therefore is rejected under the same rationale.

28. With regard to Claim 27, Claim 27 is similar in scope to Claim 6, and therefore is rejected under the same rationale.

29. Thus, it reasonably appears that Barilovits describes or discloses every element of Claims 1-8, 10, 11, 14-19, 22-24, and 26-27 and therefore anticipates the claims subject.

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

32. Claims 9, 20, 21, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barilovits (US 20020145610A1) in view of Miller (US006327304B1).

33. With regard to Claim 9, Barilovits is relied upon for the teachings as discussed above relative to Claim 1.

However, Barilovits does not teach that smooth shading of the image data is performed before the linear-output gamma translator translates the received image data into a substantially linear gamma space. However, Miller describes that smooth shading of the image data is performed (*in the prior art, areas with smooth shading gradations have regions of uniform shade, and transitions from one shade to the next are obvious*, Col. 1, lines 59-62; *decoding range will be substantially constant over the entire set of possible values*, Col. 6, line 63-Col. 7, line 5; *at block 24, a logarithmic or other correction can be performed so that the random deviation will be constant over the entire range of possible pixel values*, Col. 7, lines 25-27) before the linear-output gamma translator translates the received image data into a substantially linear gamma space (*if a correction took place at block 24, an inverse correction is performed on O at optional correction block 36*, Col. 7, lines 51-52).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Barilovits so that smooth shading of the image data is performed before the linear-output gamma translator translates the received image data into a substantially linear gamma space as suggested by Miller because Miller suggests that this is done so that transitions from one shade to the next are not obvious and to avoid making the image muddy and lacking in detail (Col. 1, lines 50-65; Col. 6, line 63-Col. 7, line 5).

34. With regard to Claim 20, Barilovits does not teach the step of performing other rendering before the step of translating the received image data to substantially linear gamma space. However, Miller describes the step of performing other rendering (Col. 1, lines 50-65; Col. 6, line 63-Col. 7, line 5; Col. 7, lines 25-27) before the step of translating the received image data to a substantially linear gamma space (Col. 7, lines 51-52). This would be obvious for the same reasons given in the rejection for Claim 9.

35. With regard to Claim 21, Barilovits does not teach that the other rendering comprises smooth shading. However, Miller describes that the other rendering comprises smooth shading (Col. 1, lines 50-65). This would be obvious for the same reasons given in the rejection for Claim 9.

36. With regard to Claim 28, Barilovits describes that the input gamma translator translates the received image data into a substantially linear gamma space, and when the input gamma translator is converting from R'G'B' to YCbCr, it adds bits [0018]. Therefore, the input gamma translator translates the received image data into a higher bit representation.

However, Barilovits does not teach that the processor core further includes a smooth shading function, and wherein the smooth shading function is performed on the image data before the input gamma translator translates the received image data into a substantially linear gamma space. However, Miller describes that the processor core further includes a smooth shading function and wherein the smooth shading of the image data is performed (*in the prior*

art, areas with smooth shading gradations have regions of uniform shade, and transitions from one shade to the next are obvious, Col. 1, lines 59-62; *decoding range will be substantially constant over the entire set of possible values*, Col. 6, line 63-Col. 7, line 5; *at block 24, a logarithmic or other correction can be performed so that the random deviation will be constant over the entire range of possible pixel values*, Col. 7, lines 25-27) before the linear-output gamma translator translates the received image data into a substantially linear gamma space (*if a correction took place at block 24, an inverse correction is performed on O at optional correction block 36*, Col. 7, lines 51-52). This would be obvious for the same reasons given in the rejection for Claim 9.

37. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barilovits (US 20020145610A1) in view of Kurihara (US 20030184551A1).

Barilovits is relied upon for the teachings as discussed above relative to Claim 1. Barilovits describes that the processor core includes anti-aliasing logic (*signal processor can be used as a graphics anti-aliasing filter by having it process 2-D and 3-D computer graphics images before they are written to the primary display buffer*, [0024]) and video merge logic (video overlay system, [0026]), and wherein anti-aliasing and video merge are performed on the image data in the substantially linear gamma space (*two and three dimensional graphics images are computed in a non-gamma corrected linear color space*, [0015], *YCbCr color spaces are derived from gamma corrected R'G"B' color spaces by a linear transformation*, [0018], *filtering YCbCr components, [0235], writing destination images to memory*, [0238])

However, Barilovits does not teach that the processor core includes alpha blending logic, wherein alpha blending is performed on the image data in the substantially linear gamma space. However, Kurihara describes the processor core (184, Figure 5) includes alpha blending logic [0084], wherein alpha blending is performed on the image data in the substantially linear gamma space (*texture filter 170 may perform bilinear, trilinear, or quadlinear interpolation*, [0081]).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Barilovits so that the processor core includes alpha blending logic, wherein alpha blending is performed on the image data in the substantially linear gamma space as suggested by Kurihara because Kurihara suggests that alpha blending must be done in linear gamma space so that it can interpolate the data used for alpha blending [0081]. Alpha blending is needed to create the effect of transparency [0077].

38. Claims 13 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barilovits (US 20020145610A1) in view of Tidwell (US006760036B2).

39. With regard to Claim 13, Barilovits is relied upon for the teachings as discussed above relative to Claim 1. Barilovits describes when the linear-output gamma translator is converting from R'G'B' to YCbCr, it adds bits [0018]. Therefore, the linear-output gamma translator additionally converts the received image data into a higher bit representation. The non-linear-output gamma translator additionally converts the received graphics data into a lower bit representation [0032, 0033], and wherein the higher bit representation comprises an 8 bit

representation and wherein the lower bit representation comprises a 5 or 6 bit representation (*five and six-bit components of these formats are converted to 8-bit values*, [0134]).

However, Barilovits does not teach that the higher bit representation comprises a 12-14 bit representation. However, Tidwell describes that calculations are done to 12 bits internally, but only 8-bits per color component are delivered out of the chip to the frame buffer, and so the pixel data width is extended to 12 bits (Col. 3, lines 36-53).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the device of Barilovits so that the higher bit representation comprises a 12-14 bit representation as suggested by Tidwell because Tidwell suggests that the pixel data width must be extended to 12 bits because calculations are done on 12 bit data, but only 8-bits per color component are delivered out of the chip to the frame buffer (Col. 3, lines 36-53).

40. With regard to Claim 25, Claim 25 is similar in scope to Claim 13, and therefore is rejected under the same rationale.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

UChauhan
ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER